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In the Claims:

1. (Currently Amended) A method of fabricating a semiconductor device in a substrate, the method comprising:

forming a trench having sidewalls and a bottom formed within the substrate, the sidewalls and bottom of the trench being formed of the substrate material;

forming a vertical silicon layer along the sidewalls of the trench to continuously cover at least a portion of the sidewalls, the vertical silicon layer laying conformally along the vertical sidewalls of the trench and having exposed vertical interior surfaces; the silicon layer not having a continuous crystalline structure; and

performing gas phase doping upon the exposed vertical interior surfaces of the vertical silicon layer so that the silicon layer is doped with a dopant having a concentration of at least $1x10^{19}$ atoms/cm^3.

2. (Original) The method of claim 1, wherein the silicon layer comprises amorphous silicon.

3. (Original) The method of claim 1, wherein the silicon layer comprises polysilicon.

4. (Original) The method of claim 1, wherein the silicon layer is at least 8 nm thick.

5. (Original) The method of claim 1, wherein the gas phase doping is performed at a temperature between about 850-1000°C, and forming the silicon layer is performed at a temperature less than the gas phase doping.

6. (Original) The method of claim 1, wherein the gas phase doping is performed at a pressure of between 1-100 Torr.

7. (Original) The method of claim 1, wherein the dopant is arsenic.

8. (Original) The method of claim 7, wherein the gas phase doping uses AsH_3 as a dopant precursor.

9. (Original) The method of claim 1, wherein the dopant is phosphorous.

10. (Original) The method of claim 1, wherein the gas phase doping is performed at a temperature between 850-950°C and a pressure of between 15-30 Torr.

11. (Original) The method of claim 10, wherein the dopant is arsenic formed by an AsH_3 precursor.

12. (Original) The method of claim 11, wherein the precursor is flowed at a rate of 100-300 sccm in the presence of H_2 for between 5-120 minutes.

13. (Original) The method of claim 11, wherein the precursor is flowed at a rate of 100-300 sccm in the presence of He for between 5-120 minutes.

14. (Original) The method of claim 1, wherein forming the silicon layer and performing the gas phase doping comprise an in-situ process.

15. (Original) The method of claim 1, wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

16. (Original) The method of claim 15, further comprising performing a wet clean of the substrate before performing the gas phase doping, wherein the wet clean removes a native oxide on the silicon layer.

17. (Original) The method of claim 1, further comprising substantially filling the trench with a fill material after performing the gas phase doping.

18. (Currently Amended) A method of fabricating a semiconductor device in a substrate, the method comprising:

forming a trench having sidewalls and a bottom within the substrate, the sidewalls and the bottom of the trench being formed of the substrate material;

lining the sidewalls with a node dielectric and forming sidewalls of the node dielectric;

depositing a vertical silicon layer to continuously cover at least a portion of the sidewalls of the node dielectric, the vertical silicon layer laying conformally along the vertical sidewalls and having an exposed interior surface; the vertical silicon layer not having a continuous crystalline structure; and

performing gas phase doping in a reaction chamber by:

flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm,

heating the reaction chamber to a temperature of between 850-1000°C, and

pressurizing the reaction chamber to a pressure of between 1-100 Torr, wherein the gas phase doping results in the silicon layer being doped with a dopant having a concentration of at least $1x10^{19}$ atoms/cm^3.

19. (Original) The method of claim 18, further comprising substantially filling the trench with amorphous silicon after performing the gas phase doping.

20. (Original) The method of claim 18, wherein the silicon layer comprises amorphous silicon.

21. (Original) The method of claim 18, wherein the silicon layer comprises polysilicon.

22. (Original) The method of claim 18, wherein the silicon layer is at least 8 nm thick.

23. (Original) The method of claim 18, wherein the dopant is arsenic or phosphorous.

24. (Original) The method of claim 18, wherein depositing the silicon layer and performing the gas phase doping comprise an in-situ process.

25. (Original) The method of claim 18, wherein depositing the silicon layer and performing the gas phase doping comprise an ex-situ process.

26. (Original) The method of claim 25, further comprising performing a wet clean of the substrate before performing the gas phase doping, wherein the wet clean removes a native oxide on the silicon layer.

27. (Original) The method of claim 26, wherein the dopant has a concentration of at least $5x10^{19}$ atoms/cm^3.